REMARKS/ARGUMENTS

This Application is in response to an Office action dated November 26, 2003. In the Office Action, claims 1-6 and 8-23 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,073,243 (Dalvi) and claim 7 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dalvi in view of U.S. Patent No. 5,944,821 (Angelo). Applicant respectfully traverses the rejections under 35 U.S.C. §§102(e) and 103(a).

I. Drawing Objections

Figures 1-5 were objected to by the draftsperson. Applicant has corrected these drawings, which are submitted herewith. Applicant respectfully requests the Examiner to withdraw the outstanding objection.

II. Rejection Under 35 U.S.C. §102(e)

Claims 1-6 and 8-23 were rejected under 35 U.S.C. §102(e) as being anticipated by Dalvi. Applicant respectfully submits that a *prima facie* case of anticipation has not been established because Dalvi fails to teach each and every element set forth in independent claims 1, 9, 14 and 18. As the Examiner is aware, "[a] claim is anticipate *only if each and every* element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987) (Emphasis added). Applicant respectfully requests reconsideration of the §102(e) rejection.

In particular, Applicant respectfully submits that an "override disable pin" is not disclosed in Dalvi. Therein, on column 2, lines 51-53 of Dalvi, block lock-bits for each memory block are described. It is contemplated that a block lock-bit, namely a stored bit in a memory block, does not expressly or inherently describe an override disable pin. For this reason alone, a §102(e) rejection should not be maintained against independent claims 1, 14 and 18.

Moreover, Applicant respectfully submits that column 19, lines 1-15, column 23, lines 20-58 and 66-67 and column 24, lines 1-4 do not expressly or inherently describe each of the following limitations:

(1) preventing modification of a representation of a primary pass-phrase when the override disable pin is asserted, the primary pass-phrase permitting access to stored information within the electronic system (Claim 1);

(2) disabling access to the stored information despite assertion of the override pin of the integrated circuit device when an override disable pin of the integrated circuit device is asserted prior to assertion of the override pin (Claim 9);

(3) disabling placement of the electronic system into the administrator mode despite assertion of the override pin of the integrated circuit device when an override disable pin of the integrated circuit device is asserted prior to assertion of the override pin (Claim 14); and

(4) an override disable pin to disable access to the information stored within the memory despite the assertion of the override pin when the override disable pin is asserted prior to assertion of the override pin (Claim 18).

In fact, Dalvi specifically describes that the pass-phrase, apparently to be considered by the Examiner to be equivalent to the passcode of Dalvi , allows the user to override the master lock bit *without* using the high voltage pin. (Emphasis added). In other words, the passcode is a mechanism to enable the master lock-bit to override the block lock-bits without selection of any pins. This teaching is contrary to the limitations set forth in independent claims 1, 9, 14 and 18.

Therefore, Applicant respectfully requests the Examiner to reconsider the §102(e) rejection, and if the rejection is maintained, to denote what exact elements he considers to be the override disable pin, the override pin and the primary pass-phrase. Such exact information may facilitate the prosecution of the subject application.

III. Rejection Under 35 U.S.C. §103(a)

The undersigned hereby contends that U.S. Patent No. 5,954,818 is not a valid prior art reference. In accordance with 35 U.S.C. §103(c), references which may qualify as prior art under 35 U.S.C. §102(e), (f), and (g) are excluded from being used as a prior art reference. The text of 35 U.S.C. §103(c) recites that "[s]ubject matter developed by another person, which qualifies as prior art under one or more of subsections (e), (f) and (g) of §102 of this Title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time of the invention was made, owned by the same person or subject to an obligation of assignment to the same person." *See, 35 U.S.C. §103(c), MPEP §706.02(l)(1).*

Herein, the subject matter of U.S. Patent No. 5,954,818 and the claimed invention were, at the time the invention was made, both owned by Intel Corporation and subject to an obligation of assignment to Intel Corporation. An assignment of the claimed invention of the subject application has been recorded at Reel No. 010966 and Frame No. 0690 in the U.S. Patent and Trademark Office as set forth in Exhibit 1. In addition, the subject application was filed on March 31, 2000, which is less than one year from the date of issue of U.S. Patent No. 5,954,818. Hence, U.S. Patent No. 5,954,818 is not a valid prior art reference and does not obviate Applicant's pending claims.

Applicant respectfully requests withdrawal of the 35 U.S.C. §103(a) rejection.

Conclusion

Applicant respectfully believes that all claims are in condition for allowance. Allowance of the pending claims is respectfully requested at the Examiner's earliest convenience.

Respectfully submitted,

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